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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,843	12/03/2004	Jan Hoogerbrugge	NL02 0480 US	7262

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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
AYASH, MARWAN	
ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
07/20/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/516,843	HOOGERBRUGGE ET AL.	
	Examiner	Art Unit	
	MARWAN AYASH	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action has been issued in response to the amendment filed 06/16/09. Claims 1-23 are pending in this application. Applicant's arguments have been carefully considered, but are not persuasive in view of the prior art as applied to a broadest reasonable interpretation of the claims and/or moot in view of new grounds of rejection. The examiner appreciates Applicant's effort to distinguish over the cited prior art by arguing perceived differences between the claims and the cited art, however, upon further consideration and/or search, the claims remain unpatentable over the cited prior art. All claims pending in the instant application remain rejected and clarification and/or elaboration regarding why the claims are not in condition for allowance will hereafter be provided in order to efficiently further prosecution. Accordingly this action has been made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 1-23 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Robertson (US Patent # 6,892,253) in view of Myers (US Patent # 2002/0146023) further in view of Bender et al. (US Patent # 5,664,223).

With respect to **independent claims 1, 7, 12, 18** Robertson discloses a device (*Robertson - fig. 4*) for writing data elements from a coprocessor into a FIFO memory, in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said device comprising:

a first counter [*master count 251 (Robertson – abstract)*] for counting the available room in said FIFO memory;

a second counter [*remote count 252 (Robertson – abstract)*] for counting the number of data elements written into said FIFO memory;

control means [*Robertson Fig. 1, 2 ,4*] coupled to the first and second counters, wherein the control means is configured for checking said first counter for available room in said FIFO memory, for checking said second counter whether a predetermined number N of data elements have been written into said FIFO memory, for decrementing the count of said first counter and for incrementing the count of said second counter after a data element has been written into said FIFO memory [*Robertson – abstract, Fig. 1-2 & 4*]; and

output means for outputting data elements to said FIFO memory [*since remote count indicates the number of entries stored in the FIFO buffer (Robertson – abstract, Col 7 lines 48-50), means for outputting/storing data elements into the FIFO are inherent in the disclosure of Robertson's invention; see also fig. 4 of Robertson where the pipeline stages output data to the FIFO buffer 410*], wherein the output means comprises a first connection to the control means, a second connection to the FIFO memory, and a third connection to the controller, wherein the control means connects between the counters and the output means, and the output means connects between the control means and the

controller [*Robertson suggests the claimed element arrangement or orientation in Fig. 1-2, but appears not to explicitly disclose the claimed arrangement*];

wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N [*Upon allocation of N (some variable number) data items into the FIFO buffer, an output signal may be asserted when N is equal to some threshold value (Robertson – Col 5 lines 7-30)*] by incrementing of the count of said second counter after a data element has been written into said FIFO memory [*remote count 252 is incremented upon allocation of data to the FIFO (Robertson - abstract)*];

wherein said control means is adapted to issue a first call for available room in said FIFO memory to said controller [*Column 7 lines 64-67, and/or Col 5 lines 7-30*]; and

wherein said output means is adapted to forward said first message and/or said first call to said controller [*Column 7 lines 64-67, and/or Col 5 lines 7-30*].

Robertson does not **explicitly** disclose the claimed control means, output means, controller, FIFO and counter arrangement or interconnection although the claimed functionality of these elements is understood to be present in Robertson, just not in the particular order that applicant has claimed so that the claims do not extent beyond the scope of what one of ordinary skill would understand to be an obvious modification to Robertson.

In the same field of endeavor, Myers teaches a transport stream multiplexer utilizing smart FIFO meters wherein a broadest reasonable interpretation of applicant claimed functional element arrangement is disclosed (*Myers Fig. 1, 3, 9, 11*)

Therefore Robertson in view of Myers disclose wherein the output means comprises a first connection to the control means, a second connection to the FIFO memory, and a third connection to the controller, wherein the control means connects between the counters and the output means, and the output means connects between the control means and the controller [*Myers Fig. 3, 9, 11*].

Robertson in view of Myers does not **explicitly** disclose the environment in which the invention is implemented - as in the preamble of the instant claim(s) – namely a processor/coprocessor environment.

Nevertheless, in the same field of endeavor Bender teaches the implementation of a FIFO similar to the one disclosed in Robertson's invention, but in a processor/coprocessor environment (*Bender – Col 2 lines 60-67, Col 4 lines 40-59*) including a controller (*Bender - Col 5 line 19*).

Therefore Robertson in view of Myers further in view of Bender discloses all limitations of the instant claim(s).

It would have been obvious to one having ordinary skill in the art at the time of the invention to include means for performing a signaling operation when the count of a counter has been incremented by N in the invention of Robertson because it would be advantageous to signal that a fullness/emptiness threshold has been exceeded before the FIFO is actually full/empty since hardware delays and latency properties may not allow a less forgiving implementation to prevent the FIFO from overflowing/underflowing (*Robertson – Col 5 lines 7-20, abstract*). Moreover, it would be advantageous to include means for performing a signaling operation when the count of a counter has been incremented by N to assist with timing of transfer operations into/out from a FIFO memory for the purpose of achieving load balancing in the case of a plurality of FIFO memories (*this understanding is supported/evidenced by Myers – US Patent # 6,877,049 – abstract, and/or Myers – US Patent # 2002/0146023 – paragraph 0012-0013*). Lastly, it would have been obvious to one of ordinary skill in the art at the time of the invention to arrange the functional elements such that they would be interconnected as claimed and as shown in Fig. 3, 9, 11 of Myers because not only would the interconnection facilitate the proper operation of the invention, but also because the number of ways that 5 functional components may be interconnected is finite, and it would have been within the purview of a

skilled artisan to select one of several know and finite interconnections for a plurality of functional elements.

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a FIFO (as part of a decoupling mechanism) in a processor/coprocessor environment in the invention of Robertson as taught by Bender because it would be advantageous to decouple a main processor from certain operations which are cumbersome and which may be (offloaded on/assigned to) a supporting co-processor (*Bender – Col 1 lines 25-37*) thereby effecting more efficient and expedient system operation.

With respect to independent claims 12, 18 Robertson's in view of Bender invention is capable of performing the steps of the claimed method and includes all elements of the claimed device since reading and writing are symmetric operations as is well known by the applicant (paragraph [0006] of applicant's specification). Is well known to one of ordinary skill in the art that reading and writing are symmetric I/O operations such that an exemplary disclosure wherein operations are performed with respect to writing data, would render a symmetric disclosure of operations being performed with respect to reading data an obvious variant.

With respect to **dependent claim 2, 13** as applied to claim 1, 12 above, Robertson in view of Bender discloses said first message indicates that sufficient data elements have been written into said FIFO memory [*Robertson – Col 7 lines 7-30*], [*main processor on the outgoing side will move the packet into its outgoing FIFO and will inform the coprocessor by putting a message into its memory (Bender - Col 10 lines 16-18)*].

With respect to **dependent claims 3, 8, 14, 19** as applied to claims 2, 7, 13, 18 above, Robertson in view of Bender discloses incrementing a write pointer, when data elements were output to said FIFO memory [*When data is put into the FIFO, the tail pointer is incremented and when data is taken out of the FIFO the head pointer is incremented (Bender - Col 10 lines 39-42)*].

With respect to **dependent claims 4, 9, 15, 20** as applied to claims 3, 8, 14, 19 above, Robertson in view of Bender discloses performing a wrap-around test after said write pointer was incremented [*check to see if the tail pointer (+2) is not equal to the header pointer (Bender - Col 11 lines 4-6)*].

With respect to **dependent claims 5, 10, 16, 21** as applied to claims 2, 7, 13, 18 above, Robertson in view of Bender discloses resetting said second counter after issuing said first message [*Robertson – Col 7 lines 47-62*], [*a reset device, operatively coupled to said output of the counting mechanism, for resetting the adaptor; and a reset transmitting device, operatively coupled between the reset device and the main processor for transmitting the reset condition of the adaptor to the main processor (Bender - Col 3 lines 35-40)*].

With respect to **dependent claims 6, 11, 17, 22** as applied to claims 1, 7, 13, 18 above, Robertson in view of Bender discloses issuing said first call for available room in said FIFO memory to said controller before said count of said first counter becomes zero [*Robertson – Col 5 lines 7-30*], [*it first polls the head pointer in its local memory and compares it with its cached value of the tail pointer to determine if there is space in the outgoing FIFO... checks to see if the tail pointer (+2) is not equal to the header pointer (Bender - Col 11 lines 2-6); If it is full, local polling occurs at the coprocessor. While there is polling occurring, the main processor can send a new "receive head" through the adaptor to thereby update the "receive head" in the coprocessor 22. (Bender - Col 13 lines 10-14). Note that issuing the call before the count of first counter becomes zero is understood to be functionally equivalent to setting a predetermined threshold value which indicates an almost full state for the FIFO queue and issuing the call based on the counter or pointer reaching that value*].

With respect to **dependent claim 23** as applied to claim 1 above Robertson in view of Bender discloses a Multiprocessing computer system, comprising: a FIFO memory; at least one coprocessor; a controller, a device for writing according to claim 1 [*See rejection of claim 1 above*].

Response to Arguments

5. Applicant's arguments filed 06/16/09 have been fully considered but are not persuasive in view of the prior art and/or moot in view of new ground(s) of rejection necessitated by amendment to the claims. All claims pending in the instant application remain rejected. Please note that any rejections/objection not maintained from the previous Office Action have been rectified either by applicant's amendment and/or persuasive argument(s).

6. Regarding applicant's remarks on pages 10-11 summarized on page 10 as: "the combination of Robertson, Bender, and Meyers does not teach all of the limitations of the claim because the combination of cited references does not teach output means for outputting data elements to said first-in-first-out (FIFO) memory, wherein the output means comprises a first connection to the control means, a second connection to the FIFO memory, and a third connection to the controller, wherein the control means connects between the counters and the output means, and the output means connects between the control means and the controller" [*the examiner respectfully submits that one may observe the arrangement of claimed components in at least Fig. 9 of Myers: with element 102 mapping to the claimed output means, elements 110, 108, 106, 104 mapping to the claimed FIFO(s); elements 116 and/or 114 mapping to the claimed controller, element 112 mapping to the claimed control means; and the elements within 112 – depicted in more detail in Fig. 3 of Myers mapping to the claimed counters*]

Conclusion

When responding to the office action, **any new claims and/or limitations should be accompanied by a reference as to where the new claims and/or limitations are supported in the original disclosure**.

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marwan Ayash whose telephone number is 571-270-1179. The examiner can normally be reached on Mon-Fri 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185
07/13/09

Marwan Ayash - Examiner - Art Unit 2185